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PROMISE

PROtotypes of Magnetic Imaging Systems for Europe

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Controller design v1

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Executive Summary

Deliverable D2.5 presents the controller design of the Pulsed Microwave Generator developed within the PROMISE project.

The Controller is a core subsystem for controlling the spin state of nitrogen-vacancy (NV) centers in diamond, enabling quantum sensing and magnetic imaging applications. The system must generate microwave signals in the 1.46–4 GHz range with sub-nanosecond timing precision, deterministic frequency hopping, phase continuity between bursts, and synchronized trigger outputs for external instrumentation

Two hardware solutions were evaluated: (1) an architecture based on the AD9164 RF DAC combined with the ADS7-V2 FPGA platform, and (2) a Xilinx Zynq UltraScale+ RFSoC-based solution. Although the RFSoC approach offers higher integration, the AD9164-based architecture was selected due to its significantly lower cost while fully meeting performance requirements

The chosen solution enables direct RF synthesis up to 4 GHz and operates at 10 GSPS, achieving 100 ps time resolution for burst control and frequency hopping within approximately 100–200 ps via internal NCO updates. A parametric waveform generation strategy is implemented: high-level burst parameters are transmitted from a PC to the FPGA via Ethernet, and the waveform is generated in real time using an internal NCO. This approach reduces memory usage, improves determinism, and simplifies system scalability

The design leverages existing Xilinx and Analog Devices IP cores for high-speed communication and JESD204B interfacing, limiting custom VHDL development to burst scheduling, phase control, and gating logic. The controller architecture is fully defined and provides a robust, scalable, and cost-effective foundation for the PROMISE microwave control system.

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1. General introduction

This deliverable, D2.5, presents the technical architecture proposed for implementing the pulsed microwave generator controller. The design focuses on achieving sub-nanosecond timing precision, deterministic frequency control, and flexible burst generation within the 1.46–4 GHz frequency range required for NV-center spin manipulation.

Two implementation strategies are considered for waveform generation: a sample-player architecture based on precomputed waveform data and a parametric waveform generation approach where high-level burst parameters are transmitted from a host PC to the FPGA. The latter approach is adopted as it significantly reduces memory requirements and allows real-time generation of RF bursts using internal FPGA logic and the DAC's numerically controlled oscillator.

The following subsections describe the selected architecture, the timing capabilities of the system, the implementation of burst scheduling and frequency hopping, and the mechanisms used to ensure phase continuity and silent DAC output between bursts.

The controller designed within the deliverable also considers the needs to integrate the control of the laser via an Acoustic Optic Modulator (AOM) T2.1 and the single-photon detector array T2.2.

2. Introduction to the MW Source

A Pulsed Microwave Generator (PMG) is required to control the spin state of nitrogen-vacancy centers in diamond. This PMG has to offer the following functionality:

1. The frequency band ranges from 1.46 to 4 GHz.
2. The length of each RF bursts must be defined with a time granularity smaller than 2ns.
3. There are 3 types of frames (a finite number of consecutive RF burst)
    a. No frequency hopping, all RF burst within the frame are set to the same frequency
    b. Frequency hopping. The burst within the same frame can change frequency. The time gap between two consecutive bursts with frequency hopping must be smaller than 1ms.
    c. No frequency hopping with continuous phase. All bursts are transmitted at the same frequency, but the phase remains constant from the end of each burst to the beginning of the next.
4. Output triggers generation. There must be dedicated output signals synchronized to edges of the burst to behave like triggers to control the activity of external equipment such as lasers, recording cameras, etc...
5. There is an output level range for the RF signal to be delivered to the antenna.

For this purpose, the following Hardware solutions have been identified.

- A solution based on the AD9164 from Analog Devices.
- A solution based on the XQZU48DR, from the Zynq UltraScale+ RFSoC Family.

3. Solutions Description

3.1 First Solution

The **AD9164** from Analog Devices is a high-performance, high-speed digital-to-analog converter (DAC) designed for advanced communication and signal generation applications.

The AD9164 is a **16-bit, 12 GSPS (gigasamples per second) RF DAC** that directly generates radio frequency (RF) signals without requiring additional analog upconversion stages. It is part of Analog Devices' RF DAC portfolio aimed at demanding systems such as:

- Wireless infrastructure (4G/5G base stations)
- Electronic test and measurement equipment

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- Radar systems
- Software-defined radio (SDR) platforms
- Satellite communications

Key Features:

- **16-bit resolution**
- **Up to 12 GSPS sample rate**
- Integrated **digital signal processing (DSP)** blocks, including interpolation filters
- On-chip **numerically controlled oscillator (NCO)** for digital upconversion
- JESD204B/C high-speed serial interface
- Excellent **spurious-free dynamic range (SFDR)** and low phase noise performance

The device enables direct RF synthesis up to several GHz, reducing system complexity by eliminating traditional mixers and analog intermediate frequency (IF) stages.

In short, the AD9164 is a state-of-the-art RF DAC optimized for high-bandwidth, high-dynamic-range signal generation in modern communication and instrumentation systems.

To implement a fully functional Pulsed Microwave Generator in the shortest possible development time and with minimum technical risk and cost, the proposed solution is based on the **AD9164-FMCB-EBZ RF DAC evaluation board** combined with the **ADS7-V2 FPGA development platform**. This approach leverages proven hardware platforms to avoid custom PCB development during the initial implementation phase.

AD9164-FMCB-EBZ RF DAC Evaluation Board

The AD9164-FMCB-EBZ is built around the AD9164, a 16-bit, 12 GSPS RF digital-to-analog converter designed for direct RF synthesis. The device integrates advanced digital signal processing blocks, including interpolation filters and a numerically controlled oscillator (NCO), enabling digital upconversion and direct generation of RF carriers in the multi-GHz range (Figure 1).

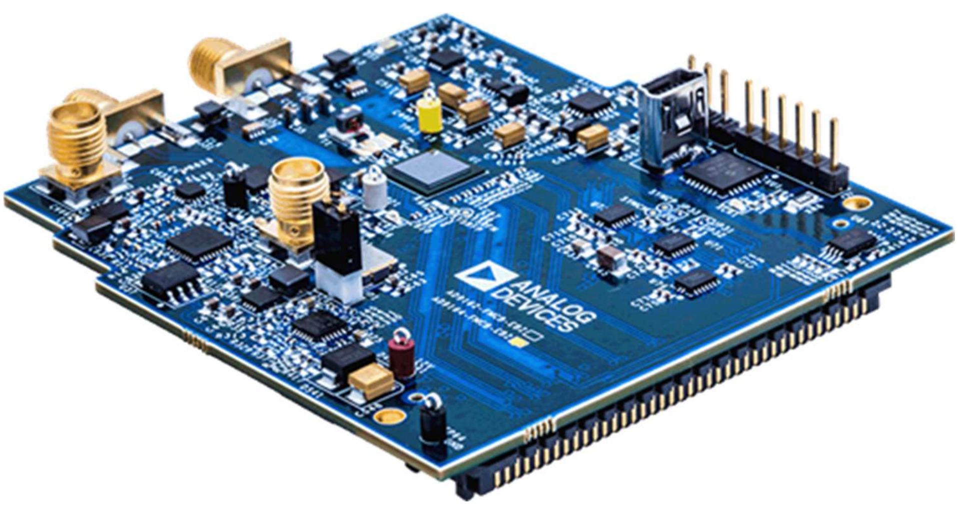

Figure 1. AD9164-FMCB-EBZ

From a system perspective, the board provides:

- A JESD204B high-speed serial interface for deterministic latency data transfer
- An FPGA Mezzanine Card (FMC) connector for direct integration with FPGA carrier boards

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- High-quality clock input circuitry supporting low phase noise operation
- Optimized RF output network for wideband signal generation
- On-board power regulation and biasing circuitry

Importantly, the Option B variant of the AD9164-FMCB-EBZ includes an RF output network tuned for a frequency band approximately spanning 1.5 GHz to 4.5 GHz, which closely matches our target operational range of 1.46 GHz to 4 GHz.

This tuning optimizes output matching, flatness, and spectral performance within this band, reducing the need for external matching networks and improving overall system efficiency for our intended microwave frequency range.

The AD9164 enables direct RF generation without requiring external mixers or IF stages, significantly simplifying the RF chain and improving spectral performance (high SFDR and low phase noise). This makes it well suited for pulsed microwave generation where signal fidelity and timing accuracy are critical.

ADS7-V2 FPGA Development Platform

The ADS7-V2 (Figure 2) serves as the digital processing and control unit of the system. It hosts a high-performance FPGA equipped with multi-gigabit transceivers capable of supporting the JESD204B link required by the AD9164.

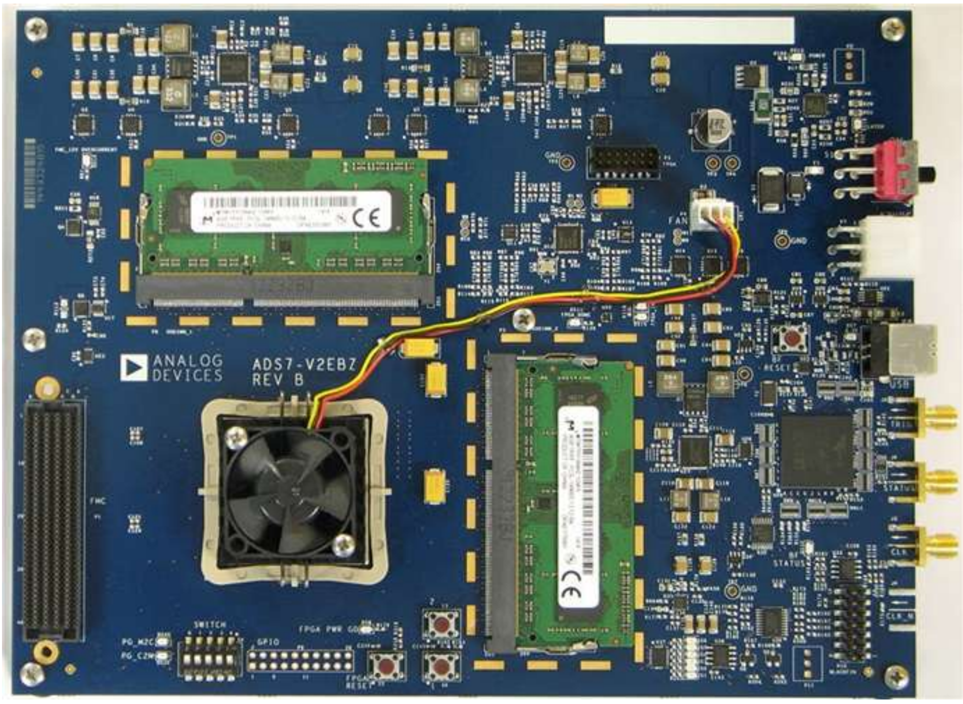

Figure 2. ADS7-V2 FPGA Development Platform

Its primary functions within the Pulsed Microwave Generator architecture include:

- Generation of high-speed baseband or IF waveform data
- Implementation of pulse shaping and timing control logic
- Management of the JESD204B transport layer
- Deterministic synchronization using SYSREF and device clock signals
- System configuration and register-level control of the AD9164

The platform provides FMC connectivity, flexible clock distribution, and sufficient programmable logic resources to implement real-time waveform generation and pulse modulation schemes.

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System-Level Architecture

In this configuration:

- The FPGA on the ADS7-V2 generates digitally modulated waveform data.
- Data is transmitted via the JESD204B interface to the AD9164.
- The AD9164 performs interpolation, optional digital upconversion, and direct RF digital-to-analog conversion.
- The resulting RF signal is available at the analog output, suitable for amplification and further conditioning.

This architecture minimizes analog complexity while maximizing digital flexibility, allowing precise control of pulse width, repetition frequency, carrier frequency, and modulation parameters.

By combining these two evaluation platforms, a robust, scalable, and high-performance pulsed microwave generation system can be implemented rapidly without the need for custom high-speed RF hardware design in the initial development phase.

It also offers up to 8 GPIOs on P9 connector for trigger generation (Figure 3), perfectly synchronized to the waveform, down to sample level.

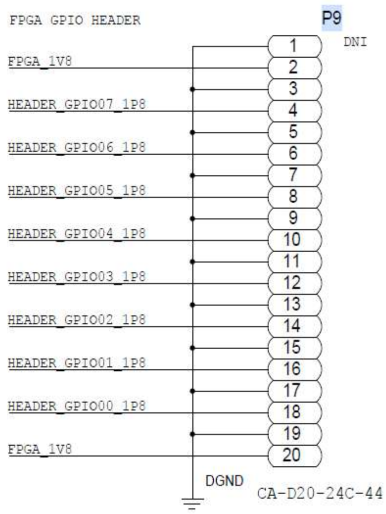

Figure 3. GPIOs connector

3.2 Second Solution

The Zynq UltraScale+ RFSoC ZCU208 Evaluation Kit, Figure 4, is a comprehensive RF development and prototyping platform designed to accelerate high-performance RF application development using the Zynq UltraScale+ RFSoC ZU48DR device. It provides out-of-the-box hardware capability for advanced signal processing, digital radio, and RF data-converter tasks with minimal custom hardware design effort.

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Figure 4. RFSoC ZCU208 Evaluation Kit

Integrated High-Performance RFSoC

- Includes the Zynq UltraScale+ RFSoC ZU48DR Gen3 device, combining a powerful processing system with programmable logic and RF data converters.
- Integrates 8 × 14-bit 5 GSPS ADCs and 8 × 14-bit 10 GSPS DACs for direct RF sampling and generation.
- Features 8 SD-FEC (Soft-Decision Forward Error Correction) cores to accelerate RF and communication workloads within hardware with reduced resource overhead.
- Unified architecture with ARM Cortex-A53 application cores, Cortex-R5 real-time cores, and UltraScale+ programmable logic supports complex mixed-signal processing.

Ready-to-Use Board-Level Infrastructure

The evaluation board provides all essential components needed for RF development:

- On-board DDR4 memory (4 GB) attached to programmable logic (PL) and DDR4 SODIMM (4 GB) attached to the processing subsystem (PS).
- Reference design mezzanine add-on cards, such as RF clocking (CLK104), loopback test (XM650), and breakout/probing cards (XM655), to reduce integration work and speed FPGA algorithm verification.
- Comprehensive board interfaces, including multiple high-speed transceivers and user I/O indicators.

Flexible I/O and Expansion

- FMC+ interface with up to 12 × 33 Gb/s GTY transceivers and dozens of differential I/O pins for custom expansion.
- Quad zSFP/zSFP+ cages allowing multiple optical or electrical high-speed links.
- Support for standard communication interfaces (USB, Ethernet, etc.) to integrate with external test equipment and host systems.

Ideal for Wideband RF & Digital Systems

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The kit enables high-bandwidth RF development spanning sub-6 GHz and extending towards mmWave IF use cases. It is suitable for advanced radar systems, wireless base stations, test and measurement platforms, software-defined radios, and adaptive radio architectures due to its:

- *Direct RF-sampling capability*, eliminating the need for external down-conversion hardware.
- High-speed data converters closely integrated with programmable logic for real-time digital signal processing.
- Scalable platform with robust processing and interface options.

Software and Design Support

- Full support with **Xilinx Vivado Design Suite**, including IP cores for RF data converters and JESD204 frameworks.
- Reference designs, tools, and documentation help jumpstart design development, simulation, and verification phases.

3.3 Selected Solution

Solution B is technically superior, and requires less VHDL development effort, but comes at a much higher cost, around 15.500€ compared to the 3000€ for Solution A. So, the solution based on the AD9164 is finally proposed.

4. Technical Proposal

4.1 Sample Player

The working scenario is for this proposal is a PC, connected to the ADS7-V2 board that controls the AD9164-FMCB-EBZ (Figure 5).

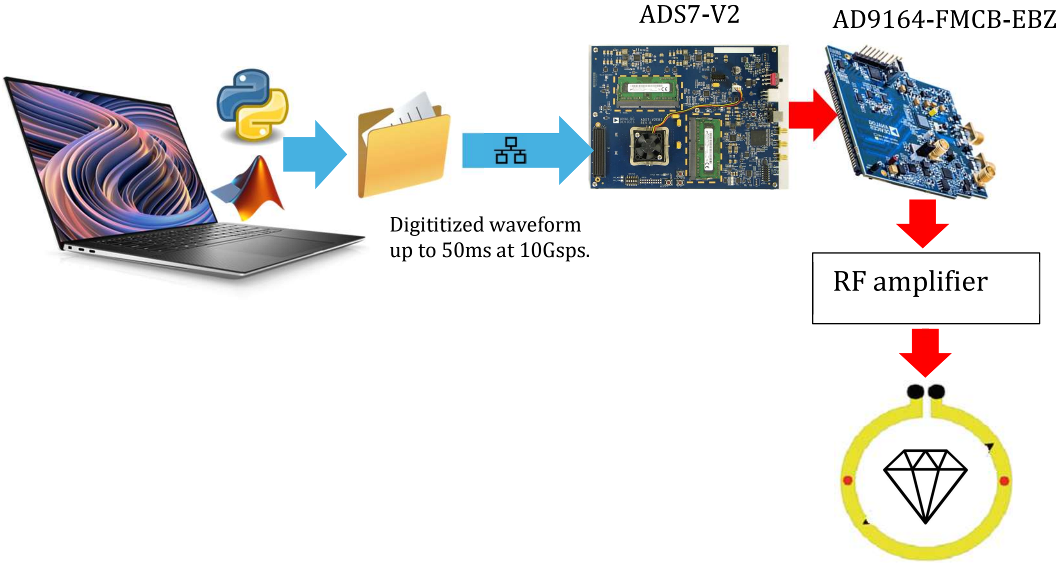

Figure 5. Sample Player

The idea is to use a PC in which generate the samples to define a specific frame, by means of Matlab or Python, then send the file via ethernet to the FPGA. Each time the memory buffer in the FPGA is full (around 50ms at a sampling rate of 10Gsps) the signal is transmitted. This way requirements such as:

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- Minimum time resolution for Burst length definition. Down to the sampling period 100ps.
- Maximum time required for a frequency hop from 1.46GHz to 4GHz. Down to the sampling period 100ps.
- Phase continuity
- DAC silent between RF burst

are ensured to sample level

This is the selected architecture as simplifies the VHDL code requirements within the ADS8-V2. In fact, all the required VHDL codes are available, as shown in the following table

Block	Custom HDL Required?	Complexity
Ethernet	Minimal	Medium
DDR3	Minimal	Low
Streaming	Minimal	Low
JESD	None	None
Burst generation	None	None
Frequency hopping	None	None

Table 1. Required VHDL codes.

There is no need to develop a large VHDL project. Most of VHDL activity is devoted to Integrating IP cores, writing small control logic, and Managing memory addressing. The difficult parts (10 GSPS timing, JESD204B, DAC synchronization) are already solved by AD reference designs.

4.2 Parametric waveform generator

In this architecture (Figure 6), the waveform is not precomputed and transferred as raw I/Q samples. Instead, a lightweight PC application (e.g., MATLAB or Python-based) sends high-level waveform parameters to the ADS7-V2 FPGA over Ethernet. These parameters include sampling rate, number of bursts, burst duration, inter-burst gaps, frequency per burst, and optional amplitude settings. The FPGA internally generates the waveform in real time using a numerically controlled oscillator (NCO) and burst control logic, eliminating the need to store large sample buffers in external memory. Communication is implemented using a standard Ethernet protocol (e.g., UDP), allowing simple, driver-free integration on the PC side. This approach significantly reduces memory requirements, removes high-bandwidth data transfer constraints, improves determinism, and enables flexible real-time control of burst-based or frequency-hopping signal generation.

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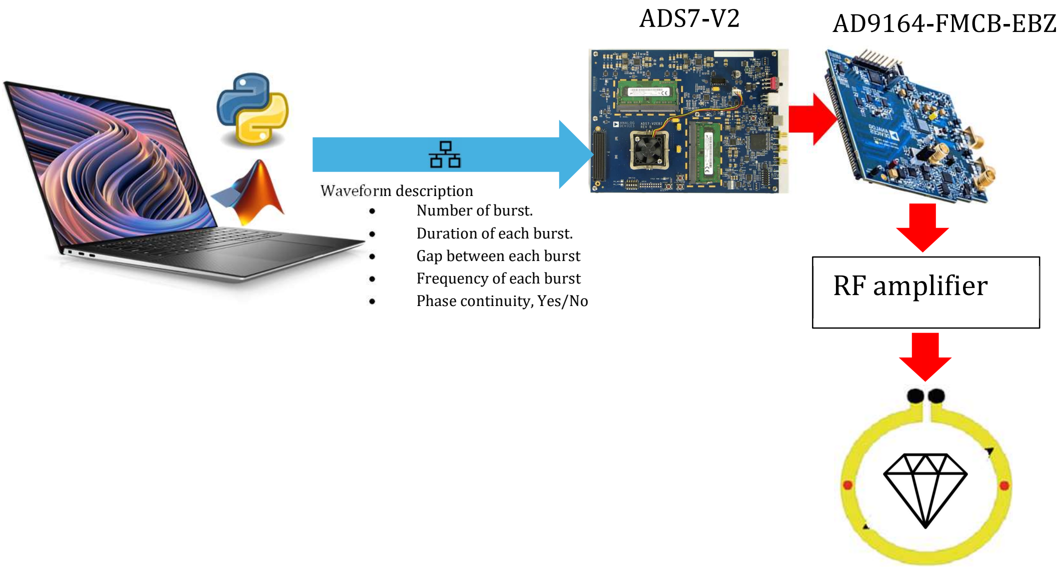

Figure 6. Parametric waveform generator

4.2.1 Minimum time resolution for Burst length definition.

If the AD9164 is operated at a 10 GSPS sampling rate for RF burst generation in the 1.46–4 GHz band, the burst duration can be defined with a time granularity equal to the sampling period (1/10 GHz), corresponding to 100 ps.

4.2.2 Maximum time required for a frequency hop from 1.46GHz to 4GHz.

For an AD9164-based RF burst generator operating at 10 GSPS, the maximum time required for a frequency hop from 1.46 GHz to 4 GHz depends on how the hop is implemented. If the hop is performed by updating the Numerically Controlled Oscillator (NCO) frequency internally within the AD9164:

- The NCO phase accumulator runs at the DAC clock (10 GSPS).
- Frequency updates are applied synchronously.
- The hop occurs at a deterministic update boundary.

The new frequency takes effect at the next internal update event, typically within 1–2 DAC clock cycles. Working at 10 GSPS, this corresponds to approximately 100–200 ps.

4.2.3 Phase continuity

There are several ways to ensure compliance with this requirement. Let us present 2 of them:

Option A: Direct Phase Control via NCO Registers

1. The AD9164 allows writing directly to NCO phase offset registers.
2. Just before starting the next burst:
    - Write the desired phase (π) into the NCO phase offset register.
    - Enable the DAC output (gate).

- This guarantees the first sample of burst i+1 starts at the exact desired phase, regardless of the off-time duration.

Option B: Use FPGA to Adjust Phase

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1. Let the NCO run free during the off-time.
2. During the off-time, compute the phase accumulated naturally:

$$\varphi_{free}= \varphi_{end\ of\ previous\ burst} + FTW\ x\ N_{off\ samples}$$

3. Apply a **phase offset** just before the next burst:

$$\varphi_{offset}= \pi - \varphi_{free}$$

This ensures the next burst starts at π, even after any length of off-time. This method is fully deterministic and works for **any gap duration**, as long as your FPGA computes and applies the offset correctly.

4.3 How to ensure the DAC keeps silent between two consecutives bursts

There also are different ways to fulfil this requirement:

4.3.1 DAC Output Gating

Use a digital enable signal from the FPGA to the DAC or JESD204B interface. When a burst ends, set DAC_enable = 0 (No samples are transmitted to the DAC output). During the gap, the NCO can continue counting internally (phase accumulator free-running) or paused depending on phase continuity requirements. And before the next burst, set DAC_enable = 1 to start transmitting samples again.

4.3.2 Practical Implementation on ADS7-V2

The DAC does not inherently “know” about burst gaps. The flow of samples can be controlled, by using a FIFO / gating logic in FPGA, stop sending samples to DAC during gap, and finally resume sending when next burst starts. This ensures no energy is output even if the NCO is still running.

4.3.3 Zero-padding.

Instead of gating, send samples with value zero to the DAC.

Regarding the VHDL effort to implement this solution:

Block	Component	Availability	Comments
Ethernet / UDP parser	Ethernet MAC (1G / 10G)	Xilinx IP	Standard AXI Ethernet MAC IP. Configure for your speed and connection type (UDP preferred).
	UDP Parser / Packet Decoder	Partially	No full IP; you typically implement a small parser to decode parameters from UDP payload. Light VHDL or HDL wrapper needed.
	Parameter Registers / AXI-Lite Interface	Xilinx IP	Can use AXI4-Lite registers to store parameters. No major modification, just map your parameters.
Burst Scheduler / Timing FSM)	Burst Scheduler FSM	No	Must be custom VHDL. Counts samples, applies burst duration and gap logic.

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	DAC Gate / Enable Logic	yes	Can implement using standard FPGA flip-flops; may wrap into the scheduler FSM.
Numerically Controlled Oscillator (NCO)	NCO / DDS IP	Xilinx IP	Xilinx provides an NCO/ DDS IP core. Can generate phase accumulator and sine/cos LUT.
	Phase Accumulator Control	no	Will need modification to allow: preloaded phase offsets, phase continuity, burst gating.
Amplitude / Envelope Control (Optional)	Multipliers / Scaling	Yes	Standard FPGA multipliers or DSP slices.
	Envelope FSM	no	Custom VHDL if you want ramping or windowing per burst.
JESD204B / DAC Interface	Multipliers / Scaling	Xilinx / Analog Devices	Xilinx and AD provide JESD204B IP. Needs to be configured for: lanes, subclass, sample width, SYSREF.
	JESD Streaming Logic	no	Only small glue logic to feed samples from NCO/envelope blocks to JESD core.
Optional Memory / FIFO Blocks	DDR / BRAM Controllers	Xilinx IP	Standard AXI4 DDR / BRAM controller cores.
	FIFO / Sample Buffer	Xilinx IP	May use FIFO for sample alignment or pipeline. Custom wrapper to connect with scheduler/NCO.

Table 2. FPGA architecture blocks showing component availability (vendor IP or custom logic) and implementation notes.

5. Conclusions

The proposed controller architecture provides a flexible and efficient solution for generating pulsed microwave signals required for NV-based quantum sensing experiments. By combining an FPGA-based control system with the high-speed AD9164 RF DAC, the design enables direct RF synthesis in the 1.46–4 GHz band while achieving a timing resolution of approximately 100 ps.

The use of a parametric waveform generation strategy allows the system to generate bursts, frequency hops, and phase-continuous signals in real time without the need to store large waveform datasets. Most of the required functionality is implemented using existing Xilinx and Analog Devices IP cores, limiting custom HDL development to relatively small control modules such as the burst scheduler and parameter decoding logic.

Overall, the architecture provides a deterministic, scalable, and cost-effective platform for pulsed microwave generation and forms a solid basis for further integration within the PROMISE magnetic imaging system. Moreover, it will be combined with the AOM that control the excitation laser included in the optical design developed in T2.1 and the single-photon detector array developed in T2.2. All subsystems will be integrated into the complete system during WP4.

6. Degree of Progress

This deliverable is a 100% complete.

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