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Executive Summary

This document presents the design and specifications of a custom Single-Photon Avalanche Diode (SPAD)-based image sensor optimized for nitrogen-vacancy (NV) diamond magnetometry imaging applications. Leveraging on low-noise SPAD technology integrated into a standard 110 nm CMOS Image Sensor (CIS) process, the sensor features a 160 ×160 pixel focal plane array for global shutter acquisition within an overall silicon area of 8.5 mm x 8.0 mm. Each pixel features a 39.2 µm pitch, a 22% fill-factor, and a reconfigurable 24-bit counter logic architecture. The design supports both continuous-wave and pulsed acquisition protocols to accommodate Optically Detected Magnetic Resonance (ODMR) and Pulsed T1-relaxometry techniques, respectively. To address the speed and dynamic range limitations of commercial cameras, the architecture incorporates two selectable readout circuits: a mixed-signal backup solution and a highly optimized, fully digital circuit operating up to 50 MHz. By utilizing a Double Data Rate (DDR) mode, the sensor achieves a full-frame readout time as low as 130 µs. Combining high dynamic range, fast time-gating capabilities (less than 5 ns), and rapid readout speeds, this sensor enhances the image signal-to-noise ratio and reduces measurement times by a factor of 10 compared to current state-of-the-art NV imaging setups.

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1. Introduction

This document reports on the design of a custom Single-Photon Avalanche Diode (SPAD)-based image sensor optimized for nitrogen-vacancy (NV) imaging applications. The design leverages advanced CMOS and SPAD technologies to develop a single-photon sensing camera, directly addressing commercial camera limitations like slow frame rates and restricted dynamic ranges, which result in lengthy measurement times. The imager is designed to be embedded within a microscope system for magnetometry applications, enabling the characterization of samples and materials by measuring magnetic fields and electrical currents with high spatial resolution and timing precision. As described in D1.2, the camera is expected to perform single-photon counting operations using either a continuous or a pulsed protocol, accommodating Optically Detected Magnetic Resonance (ODMR) and Pulsed T_1-relaxometry measurements, respectively. Figure 1 and Figure 2 illustrate the timing diagrams for both methods:

- ***Continuous protocol***: The laser source operates in continuous-wave (CW) mode, while the camera exposure is synchronized with the microwave source. In this configuration, each pixel counts the number of impinging photons within a single exposure window on the order of hundreds of microseconds (> 200 µs).

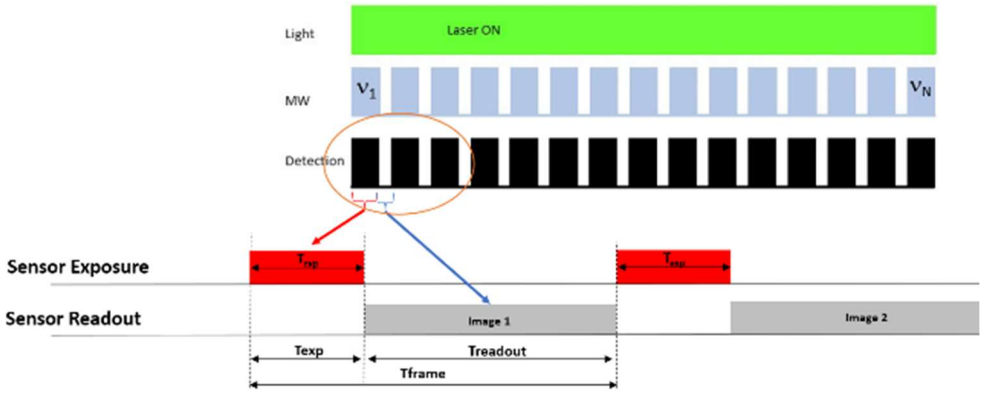

Figure 1. Continuous Acquisition Mode.

- ***Pulsed protocol***: The laser emits a sequence of pulses with a defined delay, and the camera exposure is synchronized with the microwave source during the laser initialization phase. Here, the pixel counts photons across two to four consecutive time windows (bins). Because these bins are significantly shorter than the continuous-mode windows, with Twin ranging from 300 ns to 10 µs, the sensor requires a substantially faster readout rate.

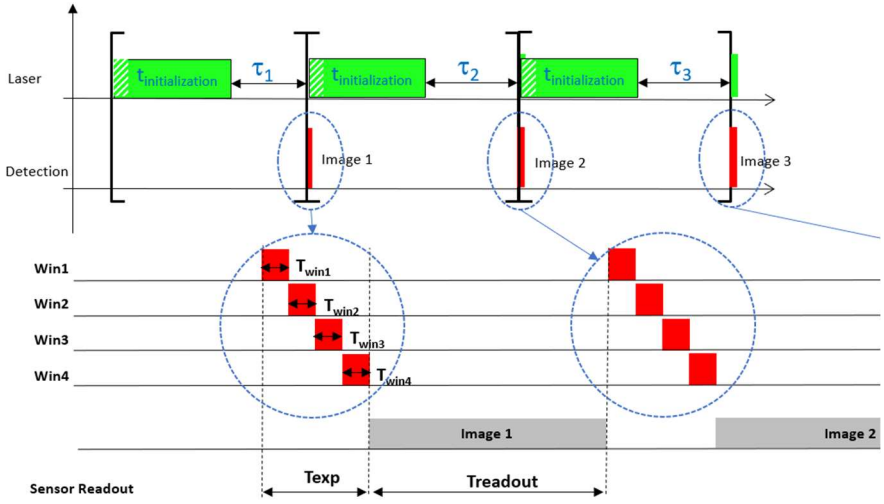

Figure 2. Pulsed Acquisition Mode.

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The measurements required by the use cases relative to the project partners along with the desired camera modes are reported in Table 1.

Partner	*Measurement Type*	*Camera Mode*
Graphenea	Magnetic field due to active current & conductivity in graphene chips	Continuous
Airbus	Magnetic field due to corrosion currents and cracks detection in alloy samples	Continuous & Pulsed
MagnetFab	Magnetic field generated by micromagnets	Continuous & Pulsed
UPVEHU	Magnetic field & properties of micro-disks & tumor cells	Continuous & Pulsed

Table 1. Camera modes suggested for each use case.

2. SPAD-Camera Design

The camera is developed using low-noise SPAD technology designed by FBK in a standard 110 nm CMOS Image Sensor (CIS) process. Figure 3 illustrates the architecture of the SPAD-based sensor developed for the PROMISE project. The focal plane array consists of 160×160 pixels designed for global shutter acquisition. At the array's periphery, a column decoder sequentially addresses the columns during the readout phase. Once a given column is selected, the pixel data are transferred to the readout circuitry and subsequently to the output pads. A Serial Peripheral Interface (SPI) allows the sensor to be programmed after startup. The control signals buffers and drivers are placed on both left and right sides of the array driving halve of the shared pixel control lines to reduce the overall line capacitance.
Figure 4 shows the layout of the PROMISE SPAD-based sensor, which occupies an overall silicon area of 8.5×8.0 mm. The input and output pads are located on the top and bottom sides of the chip, respectively. The accompanying area breakdown chart details the silicon area allocation for the main internal circuitry as well as the input/output (I/O) interfaces.

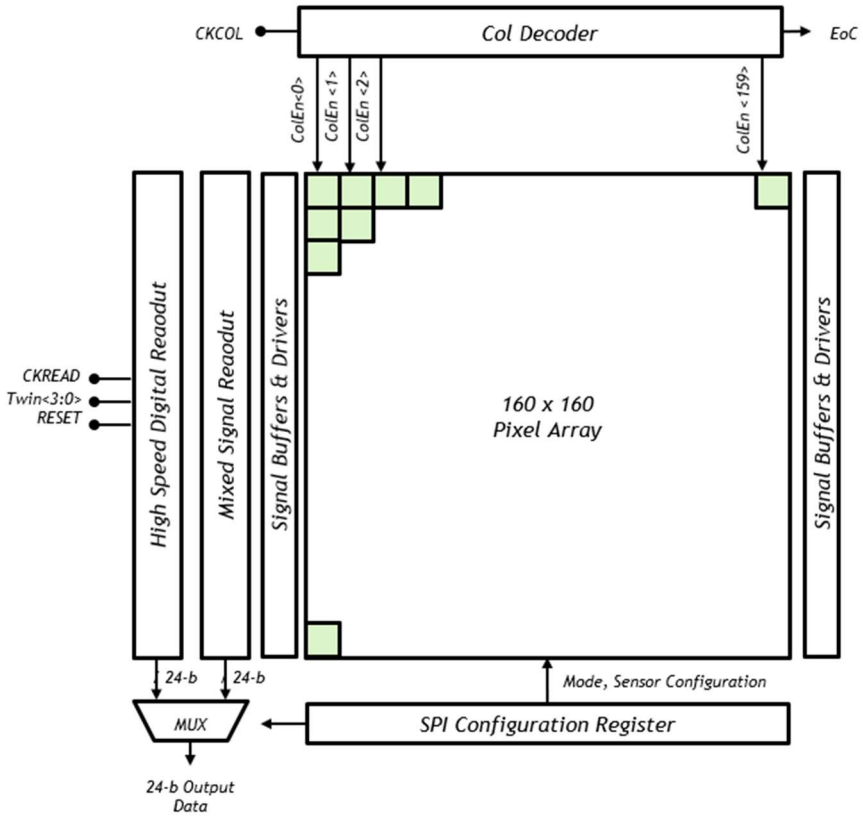

Figure 3. Architecture of the SPAD-based sensor developed for the Promise project.

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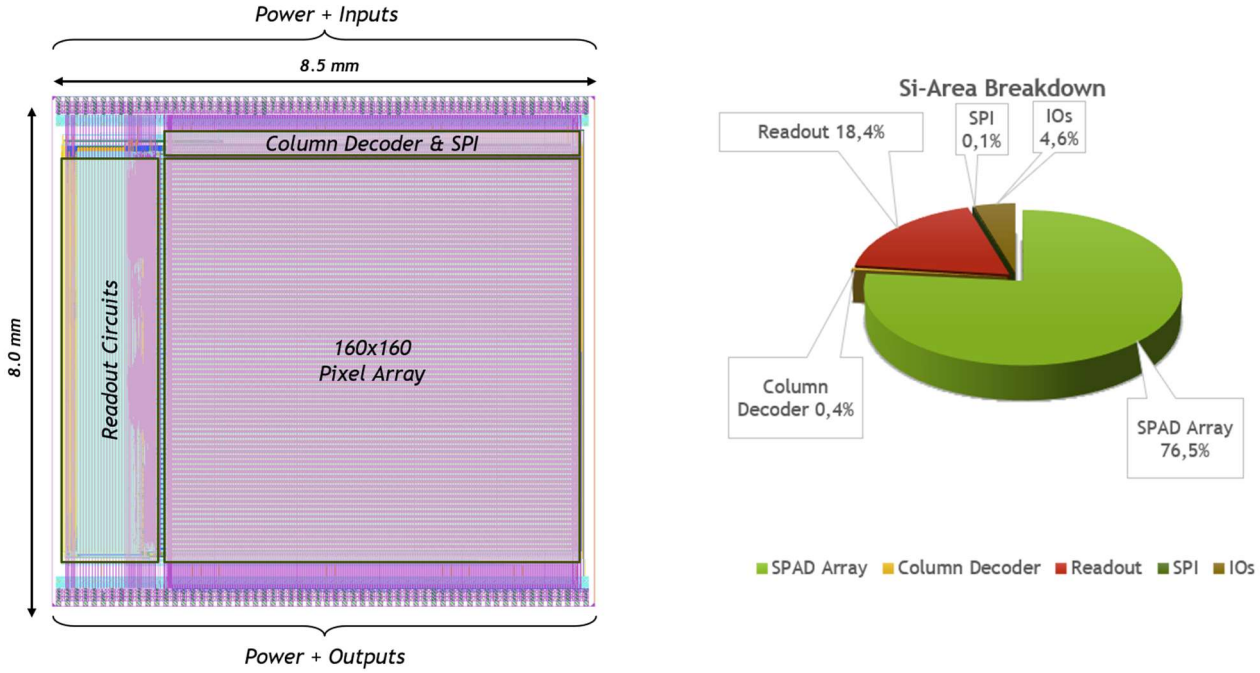

Figure 4. Left: layout of the Promise SPAD-based image sensor; right: Silicon Area breakdown

2.1 Pixel

Each individual pixel integrates a SPAD coupled with reconfigurable photon-counting electronics within a 39.2 µm pitch. The fill-factor defined as the ratio between the photon-sensitive area of the SPAD and the total pixel area is 22%. Based on previously developed SPADs fabricated using the same process [1], this yields a Photon Detection Efficiency (PDE) of 4.8% at 630 nm and maximum excess voltage. The pixel's block diagram and layout are shown in Figure 5.

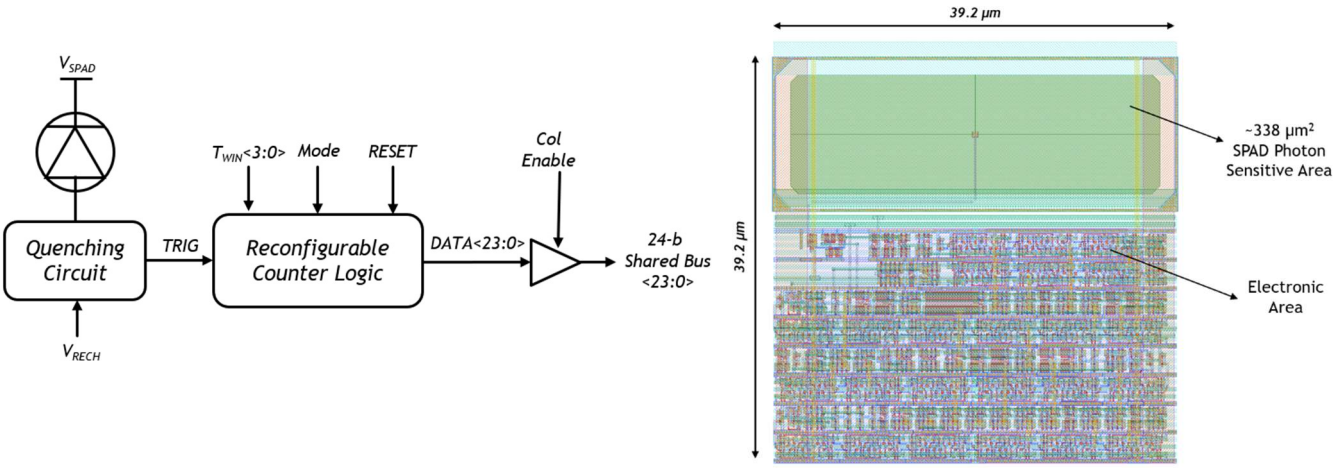

Figure 5. Pixel block diagram and layout cell view.

A configurable quenching circuit converts the avalanche current generated by an absorbed photon into a digital pulse. The duration of this pulse, known as the dead-time, can be controlled by the quenching circuit. This is achieved either by setting a fixed reference voltage or by utilizing a clocked recharge approach to optimize both power consumption and the Signal-to-Noise Ratio (SNR). The reconfigurable counter logic counts the number of pulses at the front-end output *(TRIG)* as a function of the active time bin, T_{WIN}<3:0>. The internal logic can be rearranged to accommodate single-photon counting operations with varying time bins and bit-depths. Table 2 summarizes the available hardware configurations, which can be programmed via the

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SPI configuration register. The output of the reconfigurable counter logic is connected to a shared 24-bit data bus through tri-state buffers, which are sequentially enabled by the column decoder during the readout phase.

Mode	*# bins/pixel*	*Pixel Bit Depth [bit]*	*Pixel Max Value [photons]*
#1	1-bin	24-b	16777215
#2	2-bins	12-b/bins	4095
#3	4-bins	6-b/bins	63

Table 2 . Reconfigurable Counter Logic available modes.

2.2 Readout Circuit

The sensor integrates two separate readout circuits that serve the same purpose but are implemented using two different design flows. These circuits share the same 24-bit output data bus, and only one circuit can be selected during sensor operation.

The fully digital readout circuit is implemented using digital synthesis tools. It is composed of a multiplexing and sampling stage, followed by a row sequencer block and a high-speed serializer. Once the data are sampled, the row serializer transfers them in 192-b packets to the high-speed serializer, where they are streamed to the output interface. In simulations, the circuit can operate with a readout clock (CK_{READ}) of up to 50 MHz, transferring pixel data at each clock edge. This enables a full-sensor readout in approximately 260 µs. To further increase the frame rate, a Double Data Rate (DDR) mode can be activated. This mode enables the simultaneous readout of two adjacent pixels in the same column by allocating only the 12 least significant bits (LSBs) to the shared data bus, effectively trading dynamic range for speed. Consequently, the sensor readout time is reduced to 130 µs, enabling high-speed NV imaging at approximately 7.6 kfps.

A second readout circuit, designed using a mixed-signal approach, is also included in the design to serve as a backup solution. This circuit stores the column data after it is addressed by the column decoder. The register is then scanned, conveying the pixel data to the shared 24-b data bus to be streamed out. In simulations, this circuit operates at a frequency of up to 30 MHz, resulting in a readout time of 850 µs.

3. SPAD-Camera Specifications Summary

Table below summarize the features of the developed camera sensor. The reconfigurable logic modes can be combined with the DDR option trading off dynamic range for readout speed.

Features	*From D1.2 (System specifications)*	*Design Specification*	*Motivations*
Sensor Size	*n.a.*	8.5×8.0 mm^2	
Number of pixels	≥ 200x200	160x160	Limited by the available Si-area (8.5×8.0 mm^2), the large pixel pitch (number of bits/pixel) and readout circuits.
Pixel Size	40x40 – 50x50 µm	39.2 µm	Larger number of pixels → Higher resolution
Per-pixel photon count rate	~100s of MHz	<< 25 MHz	Limited by the SPAD dead time (~10-20 ns / 50MHz) and counter depth. The laser power needs to be reduced to avoid saturation.
T_{EXP}/T_{WIN} *[3:0]*	≥ 200 us (Continuous) 300ns – 10 us (Pulsed)	User defined	

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PDE @ 630 nm	5%	4.8 %	In-pixel electronics required larger area than expected.
Tunability Texp/Twin	~ 50ns	~ 5 ns	
Minimum Texp/Twin	~100 ns	≤ 5 ns	
Number of bins	> 3	1 / 2 / 4	
Pixel Depth	> 14-b (Continuous) 8-10 b/bin (Pulsed)	1 × 24-b bin 1 × 12-b bin (×2 speed in DDR) 2 × 12-b bins 2 × 6-b bins (×2 speed in DDR) 4 × 6-b bins	
Readout time (1 frame)	~ 200 µs	Digital Ro: 260 µs / 130 µs (DDR) Mixed Ro: 850 µs	

4. SPAD-Camera System

The newly developed SPAD sensor will be integrated into a custom PCB hosting a commercial FPGA board (XEM7310) and optics support, which will be designed over the coming months while awaiting the fabrication of the camera samples. The FPGA generates the control signals for both the acquisition and readout phases of the SPAD-based camera, facilitating data collection and transfer to a host PC via a USB connection. Simultaneously, the FPGA interfaces with the external microwave source, initiating acquisition when the 1.8V camera trigger (*Trig_Camera*) is asserted, also providing the internal FPGA memory status via the *Empty* and *Full* flags.

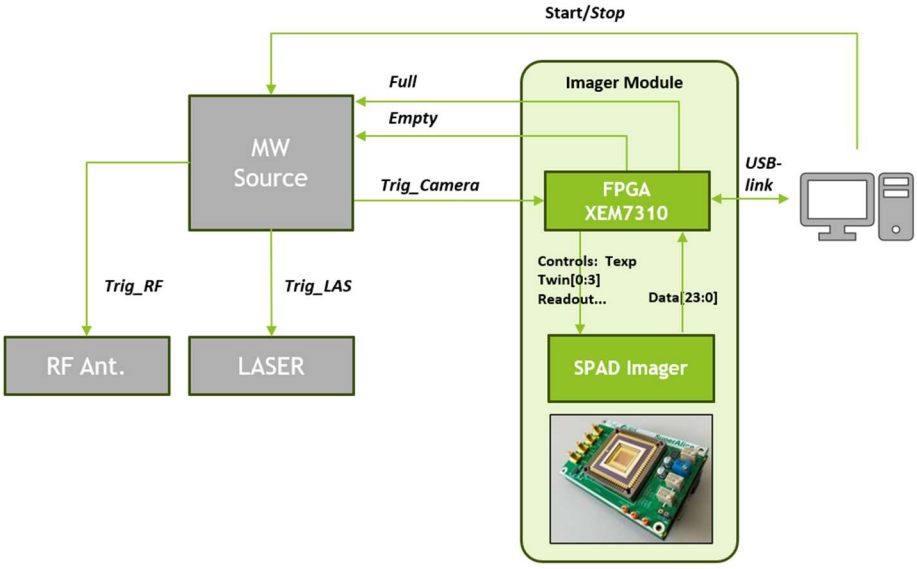

Figure 6. SPAD-camera module and interfaces with the microwave source.

5. Conclusions

This document reports the design specifications of the implemented SPAD-based image sensor specifically developed for NV imaging applications, which can be adopted for both continuous and pulsed acquisition protocols. The newly developed SPAD-based sensor is designed to improve the quality of the NV image, boosting the overall signal-to-noise ratio (SNR) due to the inherent digital nature of the SPAD detector. Because of the high pixel dynamic range (24-bit/pixel), fast time-gating capabilities (less than 5 ns), and the high-speed readout circuit (approximately 130 to 260 µs), the sensor allows for quicker and more precise acquisition compared to slower commercial cameras or general-purpose SPAD sensors with limited dynamic

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range. Combined, these performance enhancements will reduce the measurement time required in NV imaging setups by a factor of 10 compared to modern setups employing current state-of-the-art sensors.

6. Degree of progress

This deliverable is a 100% complete. At the time of writing of this document the design is complete and ready, and it is expected to be submitted to the foundry for fabrication by the end of July 2026.

7. References

[1]. Moreno-García, Manuel, et al. "Low-noise single photon avalanche diodes in a 110nm CIS technology." *2018 48th European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2018.

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